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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,488	10/12/2000	Kevin Frank Smith	SJ00-00-044	7862

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	20

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,488	SMITH, KEVIN FRANK	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-19 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 22, 2003 (Paper no. 15) has been entered.

Response to Amendment

2. This Office action is in response to the amendment filed on September 22, 2003 (Paper number 15).

Claim Objections

3. Claim 29 is objected to because of the following informalities:

Regarding claim 29, lines 1-2, "a prefetch of data into a cache a computer system" should be --a prefetch of data into a cache in a computer system--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 15-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 15 recites the limitation "the cache model" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 16 recites the limitation "the internal model" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 16-18 are also rejected because of depending on claim 15, containing the same deficiency.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 19, 28 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang (US PAT. 5,956,746).

Regarding claim 1, Wang discloses a method for scheduling pre-fetches into a cache, i.e., BSRAM array (24, figure 3) of a data storage system (50, figure 3), the method comprising remotely modeling dynamic operation of the cache (col. 3 line 1 through col. 4 line 22 and col. 5 line 2 through col. 6 line 27), the remotely modeling, i.e., predictor (54, figure 4) including

providing a model, i.e., predictor tag array (80, figure 4), of data elements currently stored within the cache, i.e., predictor tag array stores the first portion of the tag information which corresponding to the second portion of the tag information in the cache array (24, figure 3) and (col. 3 line 1 through col. 4 line 22), and making a cache management decision based upon the model, i.e., the predictor is able to decide which way is associated with the tag way information which stores in the predictor tag array and the corresponding match address in cache array (col. 5 line 45 through col. 6 line 7).

Regarding claim 2, Wang discloses the method wherein making a cache management decision comprising intercepting a request for a data element from a stream of Input/Output data request passed between a processor (52, figure 3) and a storage device, i.e., BSRAM array (24, figure 3) of the data storage system (50, figure 3), and determining whether to schedule a pre-fetch, i.e., predict, of a data element logically successive to the requested data element in accordance with contents of the cache as indicated by the model, i.e., predictor including a predictor tag array (80, figure 4) stores first portion of tag information which corresponding to the second portion of the tag information in the cache array (24) and further compare the requested address with the first portion of tag information in the predictor tag array (80), and makes cache management decision (col. 3 line 1 through col. 4 line 22 and col. 5 line 45 though col. 6 line 27).

Regarding claim 19, Wang teaches making a cache management decision comprises deciding to schedule a pre-fetch, and further comprising scheduling a pre-fetch by sending an I/O request to the cache (col. 5 line 45 through col. 6 line 49).

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 19

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-4 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US PAT. 5,956,746) in view of Tipley et al. (US Pat. 5,325,504 hereinafter Tipley).

Regarding claims 3-4, Wang differs from the claimed invention in not specifically teaching that the cache is least recently used cache or native LRU-only cache which is not substantially modified. However, it is notoriously well know in the art of using least recently used cache native LRU-only cache in order to properly reshuffle a replacement order based on read hits to a particular way, for example see Tipley (col. 2 lines 34-47 and col. 7 lines 51-65). By using least recently used cache or native LRU-only cache as taught by Tipley, it increases system efficiency of Wang by overwriting or recycling an oldest least recently used memory location in sequence. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wang in using least recently used cache or native LRU-only cache because of increasing system efficiency.

Regarding claims 22-23, the limitations of the claims are rejected as the same reasons set forth in claims 3-4.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US PAT. 5,956,746) in view of Kurokawa et al. (UP 04-367984).

Regarding claim 7, Wang teaches to determine the size of the cache (col. 4 line 34 though col. 5 line 25 and col. 6 lines 9-27). Wang differs from the claimed invention in not specifically teaching periodically fetching an I/O rate of the cache and periodically fetching a hit rate of the cache. However, Kurokawa teaches a cache control unit for periodically fetching and I/O rate of the cache and a hit rate of the cache in order to facilitate the development of a program whose cache hit ratio is high. By periodically fetching the I/O rate and the hit rate of the cache as taught by Kurokawa, it increases the cache-hit-ratio. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wang in periodically fetching and I/O rate of the cache and periodically fetching a hit rate of the cache, as per teaching of Kurokawa, because it increases the cache hit-ratio.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US PAT. 5,956,746) in view of McNutt et al. (US PAT. 5,606,688 hereinafter McNutt).

Regarding claim 8. Wang differs from the claimed invention in not specifically teaching to periodically calculating a single reference residency time (SRRT) for a data element within the cache. However, it is notoriously well know in the art of periodically calculating a single reference residency time (SRRT) for a data element within the cache, for example see McNutt

(abstract, col. 10 lines 52-65 and col. 11 lines 41-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the storage system of Wang periodically calculating a single reference residency time (SRRT) for a data element within the cache, as per teaching of McNutt, because it optimizes the efficiency with the cache controller for maintaining useful data in the cache.

12. Claims 11-14 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US PAT. 5,956,746) in view of Dixion et al. (US PAT. 4,490,782 hereinafter Dixion).

Regarding claims 11-14, Wang differs from the claimed invention in not specifically teaches to assign a priority value to the requested data command comprising the priority value assigned to the preceding data element plus one when the preceding data element is found to be present, and to determine whether to schedule a pre-fetch of a data element by comparing the priority value of the requested element with a dynamic threshold so that the requested data element is pre-fetched into the cache if the priority value of the requested data element is greater than the dynamic threshold. However, Dixion teaches cache system with pre-fetch determined by requested record's position within data block comprising the steps of assigning a priority position to a requested data element in order to determine whether to schedule a pre-fetch of a data element by comparing the priority value of the requested with dynamic threshold and pre-fetching the requested data element when the priority value is greater than the dynamic threshold (col. 15 line 46 through col. 18 line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wang in assigning a priority value to the requested data command comprising the priority value assigned to the

preceding data element plus one when the preceding data element is found to be present, and to determine whether to schedule a pre-fetch of a data element by comparing the priority value of the requested element with a dynamic threshold so that the requested data element is pre-fetched into the cache if the priority value of the requested data element is greater than the dynamic threshold, as per teaching of Dixion, because it provides a data processor with substantially increased operating speed.

Regarding claims 25-27, the limitations of the claims are rejected as the same reasons set forth in claims 11-14.

13. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US PAT. 5,956,746) in view of Weinberger et al. (US PAT. 6,453,389 hereinafter Weinberger).

Regarding claims 15-18, Wang differs from the claimed invention in not specifically teaches to periodically re-evaluating the performance of the cache model comprising the steps of determining whether the dynamic threshold used in the internal model of the cache accurately models the performance of the cache by comparing the performance of the dynamic threshold with an alternate dynamic threshold. However, Weinberger teaches the computer system comprising a pre-fetch apparatus (300, figure 4) recursively reevaluate the performance of the cache by the same determination and compare steps (col. 7 lines 16-60 and col. 16 lines 6-52). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the storage system of Wang in the pre-fetch method of periodically re-evaluating the performance of the cache model comprising the steps of determining whether the dynamic threshold used in the internal model of the cache accurately

models the performance of the cache by comparing the performance of the dynamic threshold with an alternate dynamic threshold, as per teaching by the computer system of Weinberger, because it minimize the data missed of the memory accessing operation and prevent the computer system stalls.

14. Claims 21, 29-30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US PAT. 5,956,746).

Regarding claim 21, Wang discloses a data pre-fetch scheduling system (50, figure 3) comprising a cache, i.e., BSRAM array (24, figure 3) configured to communicate with a processor (col. 3 line 56 through col. 3 line 15), and a remote pre-fetch module, i.e., predictor (54, figure 4) configured to communicated with the host and the cache and configure to determine whether to schedule a pre-fetch of data into the cache (col. 3 line 1 through col. 4 line 22 and col. 5 line 2 through col. 6 line 27), and a modeling module, i.e., predictor tag array (80, figure 4)operating within the remote prefetch module configured to model the cache, including providing a model of data elements currently stored within the cache, i.e., predictor tag array stores the first portion of the tag information which corresponding to the second portion of the tag information in the cache array (24, figure 3) and (col. 3 line 1 through col. 4 line 22). Although Wang does not clearly teaches a host in the processor (52), Wang teaches the predictor (54) with corresponding predictor tag array (80), cache controller (58, figure 3) and so as other components are both resided within the processor (52) (figure 3 and col. 7 lines 14-25), and it is notoriously well known in the art that the processor (52) is having a host or CPU to generate a requested data/instruction to the predictor for performing a predict and/or pre-fetch operation

before it really access to the cache array (24). Therefore, it recognizes the processor (52) having a host/CPU to generate or initialize a request and/or memory access to the predictor (54) and cache array (24).

Regarding claim 29, Wang discloses a pre-fetch module, i.e., predictor (54, figure 4) for determining whether to schedule a pre-fetch of data into a cache, i.e., BSRAM array (24, figure 3) in a computer system (50, figure 3), the pre-fetch module comprising a modeling module configured to model dynamic operation of the cache (col. 3 line 1 through col. 4 line 22 and col. 5 line 2 through col. 6 line 27), wherein the modeling module is further configured to provide a model, i.e., predictor tag array (80, figure 4) of data elements currently stored within the cache, i.e., predictor tag array stores the first portion of the tag information which corresponding to the second portion of the tag information in the cache array (24, figure 3) and (col. 3 line 1 through col. 4 line 22), and a calculation module, i.e., comparator (94, figure 4) configured to made a cache management decision based upon the model (col. 3 line 1 through col. 4 line 22 and col. 5 line 45 though col. 6 line 49). Although Wang does not clearly discloses the pre-fetch module comprising a modeling module, Wang teaches the on-processor predictor is able to perform a pre-fetching function before the request to the cache array (24) by receiving and generating the requested tag information from the processor and making decision via the result from the comparator (94) based on the tag information stores in the predictor tag array (80). Therefore, it recognizes the pre-fetch module having a modeling module to receiving requested data from processor and generating the requested data to the predictor tag array to perform the pre-fetching operation.

Regarding claim 30, the limitations of the claim are rejected as the same reasons set forth in claim 29.

Regarding claim 32, the limitations of the claim are rejected as the same reasons set forth in claim 21

Allowable Subject Matter

15. Claim 20 is allowed.

Response to Arguments

16. Applicant's arguments with respect to claims 1-19 and 21-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kahle et a. (US PAT. 6,460,115) discloses system and method for pre-fetching data to multiple levels of cache including selectively using a software hint to override a hardware pre-fetching mechanism (abstract).

Johnson et al. (US PAT. 5,845,101) discloses pre-fetch buffer for storing instructions prior to placing the instructions in an instruction cache (col. 2 line 49 through col. 3 line 47).

Kedem et al. (US PAT. 6,134,643) discloses method and apparatus for cache line prediction and pre-fetching using a prefetch controller and buffer and access history (abstract).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li
Art Unit 2186

11/3/03

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2100